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Accurate Interleaved Sampling of Repetitive Ultrasonic Waveforms: Two Clock Timing Architecture and its FPGA Implementation

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Abstract *–Random interleaved sampling has become a widespread operating mode for digital storage oscilloscopes. Different repetitions of (notionally) the same waveform are recorded at random time shifts, and are interleaved in memory. This procedure requires substantial time, especially if further averaging is required. In this paper an approach that ensures accurate time shifts is presented for ultrasonic measurements. Operating two independent oscillators with related frequencies forms the accurate shifts. One of these is used to excite an ultrasonic transducer, and the other to clock the analogue to digital converter (ADC). This architecture was implemented using a commercial "off-the-shelf" Field Programmable Gate Array (FPGA). An experimental waveform is presented that was sampled at the equivalent sampling frequency of 2160 MHz using an ADC with a clock frequency of 80 MHz. Power dissipation related to different architectures is discussed.*

Keywords *– waveform measurement, ultrasonic instrumentation, accurate interleaved sampling, two clock timing architecture*

I. INTRODUCTION

Ultrasonic imaging techniques are well established in medical diagnostics, flaw detection and imaging in the context of large engineering structures [1]. Applications of ultrasound to material evaluation are also well established and there is growing interest in the use of similar methods to monitor chemical phenomena both in the laboratory and in-process [1-2]. The traditional approach for digitizing ultrasonic waveforms, using a single high speed ADC becomes non viable for novel transducers/systems operating at above 100 MHz because of the high cost involved and specific expertise required. Numerous examples of these applications are presented every year, based either on laser ultrasound, cMUT or pVDF devices [3]. This requires further development of alternative architectures for high speed digitizing in ultrasonic instruments.

Interleaving presents an architectural possibility of improving the equivalent sampling frequency of data acquisition system by up to an order of magnitude and more. A great deal of attention is paid at the moment to development and analysis of systems containing several ADCs that substitute a single high-speed ADC operating in real time (e.g., [4,5], fig.1, captions on the left). The inherent disadvantages of this approach are the increase in cost of components and their interconnection compared to a single low speed ADC, and analysis/prevention/compensation for inaccuracies appearing due to differences in parameters of different ADCs used. In spite of these, ADC interleaving could be cost effective or even the only possible solution for sampling non-repetitive waveforms due to the high cost or unavailability of a single ADC solution.

Both disadvantages of ADC interleaving could be avoided if the sampled waveform is repetitive (or can be excited repeatedly). In this case a single low speed ADC can be employed for different repetitions (frames) of the waveform of interest with different time offsets, resembling ADC interleaving (fig.1). The inherent disadvantage here is the inability to sample non-repetitive waveforms (e.g., communication signals) in real time. However for some applications like wave remote sensing (e.g., ultrasonic NDE/NDT, active radar and sonar imaging and range finding) it is possible to excite (notionally) the same waveforms over and over again if the repetition frequency is relatively high and/or movement of targets is relatively slow.

Frame interleaving is often used to improve temporal resolution of digital storage oscilloscopes (DSOs). Random interleaved sampling (RIS) involves digitising several waveforms, accurate measurement of a time difference between an external trigger event and the nearest edge of an internal DSO ADC clock, and interleaving the acquired waveforms according to their position in the time domain [6]. The disadvantage of the method becomes evident if high-resolution acquisition is required and/or averaging is involved. In this case a complete acquisition requires a significant amount of time due to inherent randomness of the RIS. On the other hand, if the waveform of interest can be excited at will, it is possible to achieve a small frame jitter for the acquired waveform [7], and employ accurate interleaved sampling (AIS). The number of frames required to complete acquisition would be exactly equal to the interleaving factor (fig.1) - a significant advantage over the RIS. The price AIS pays for the increase in temporal resolution comparing to ADC interleaving or a single ADC is the proportional increase in measurement time.

AIS could in principle be implemented by using a multi-phase clock oscillator designed for ADC interleaving. Unfortunately existing ASICs remain proprietary (e.g., [8]). Building these oscillators from digital electronic components would require high internal clock frequencies, which rules out convenient commercially available reconfigurable logic devices. The aim of our development was to implement scalable AIS using commercially available FPGAs.

This paper describes results of developing a frame interleaved AIS data acquisition architecture for an ultrasonic

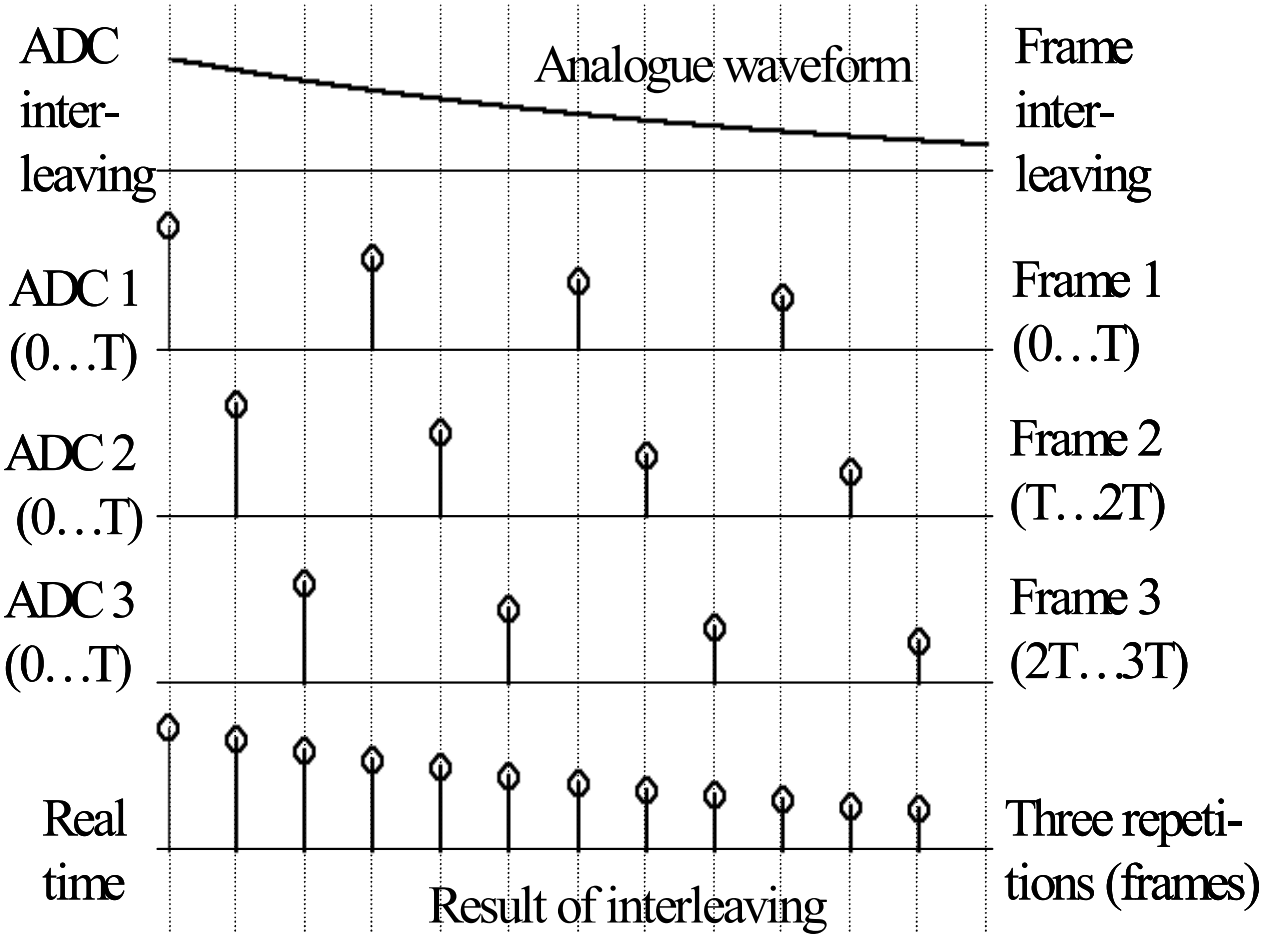

Fig.1. Illustration of 3-fold interleaving (on the left – ADC interleaving, on the right – AIS interleaving)

instrument, its implementation using commercially available FPGA technology and design tools, presents examples of acquired waveforms, and discusses the power dissipation related to AIS.

II. USING TWO OSCILLATORS WITH RELATED FREQUENCIES FOR ACCURATE TIMING

In the majority of ultrasonic systems a transmitting device is excited periodically and the resulting ultrasonic wave passes into the test medium and is ultimately captured by a receiving device, amplified, digitized and subsequently processed. The repetitive nature of the operation provides the basis for efficient designs of synchronous data acquisition architecture.

Let us consider two oscillators whose frequencies precisely satisfy the following relationship

$$M_1 f_1 = M_2 f_2, \tag{1}$$

where $M_1 \in N$, $M_2 \in N$, $M_1 = M_2 + 1$. This condition implies that if the rising edges of the oscillators coincided at some instant t_0 they would *exactly* coincide again at

$$t_k = t_0 + k\frac{M_1}{f_2} = t_0 + k\frac{M_2}{f_1}, \quad k \in N. \tag{2}$$

It makes it possible to predict when the oscillators will have their rising edges coincident again by counting their pulses to M_1 (for f_2) and to M_2 (for f_1). By using one clock sequence for excitation, and the other for sampling, it is possible to produce exactly the same waveforms many times.

Two clock timing architecture assumes that the first repetition (frame) will be excited when the rising edges of both clocks coincide, but the following waveforms will be excited by the successive pulses. This is illustrated in fig.2 for sampling an exponentially decaying pulse stimulated by different successive rising edges of clock f_2. At the first repetition of the excitation the edges of the clocks coincide with each other (frame 1, fig.2). The first pulse of f_2, shown in fig.2 triggers the excitation. The ADC samples an input

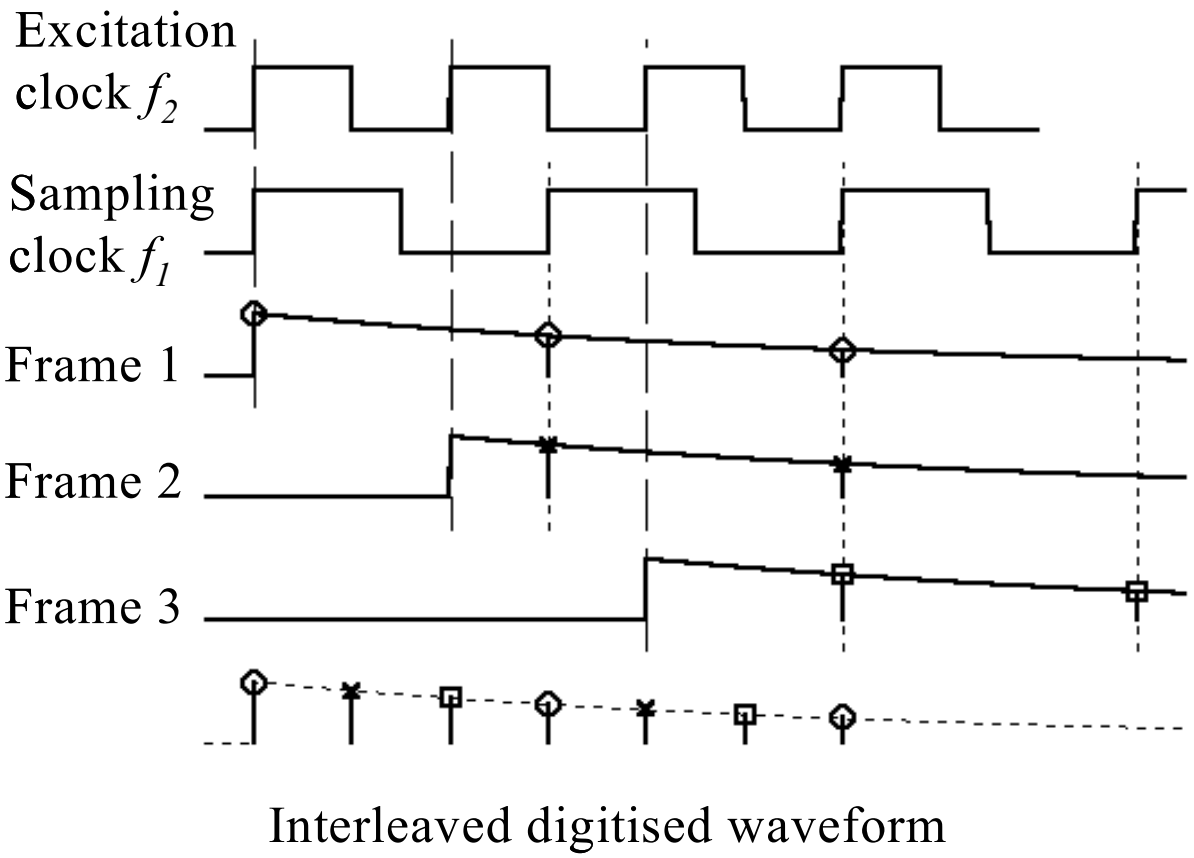

Fig.2. Operation of two clock architecture for the clock ratio 2:3 (dashed lines – excitation of a particular frame, dotted lines – sampling instants)

signal with zero delay relative to the edge of the excitation pulse. At the second repetition the excitation trigger is associated with the second pulse of f_2. The ADC starts sampling after the excitation trigger from the second pulse of f_1. This ensures a delay between the excitation and the sampling sequence of $1/f_1$-$1/f_2$ (frame 2). At the third repetition the third pulse of f_2 triggers the excitation pulse. The ADC is clocked with the delay of $2\times(1/f_1-1/f_2)$ to the excitation trigger, that is frame 3. The acquired samples are interleaved in RAM, and the RAM address is incremented by M_1 (rather than 1) for every successive sample in the same frame; the addresses in every successive frame are offset from the previous frame by 1. After the acquisition of the last frame (3rd frame in fig.2) this offset is reset to 0. The acquisition therefore could continue from frame 1 synchronously thereby enabling, if desirable, accurate on-the-fly averaging [9]. Averaging is routinely used in ultrasonic measurements to reduce the uncertainty of the acquired data (e.g., [10]).

Two clock sampling architecture is employed for acquisition of a single sample per frame only in on chip oscilloscopes [11]. This limits the application of the technique to cases where few samples are to be collected at high repetitions rates. For example, the ultrasonic signal presented in fig.4 consists of 2160 samples for 1 mks at the equivalent sampling frequency of 2160 MHz. The signal could be excited at a maximum repetition frequency of 4 kHz in order to avoid unwanted reflections in the test medium that otherwise could overlap the response of interest. A single record without averaging required a measurement time of 27/4kHz <7 ms in our system, whilst using a single sample per frame technique would require 2160/4kHz=540 ms. In the second case the averaging used for fig.4 (1024 averages) would become impractical due to the measurement time required (more than 540 s).

III. IMPLEMENTATION OF TWO CLOCK ARCHITECTURE AND EXPERIMENTAL RESULTS

The very close synchronization that is required in this system can be achieved, for example, by using digital clock managers (DCMs) available on Xilinx FPGA chips. These DCMs are capable of generating several related and tightly synchronized clock sequences. The ADC (lower frequency, f_1) is clocked by the basic frequency obtained from an on-board low jitter oscillator, while the excitation trigger (higher frequency, f_2) is clocked by a synthesized signal,

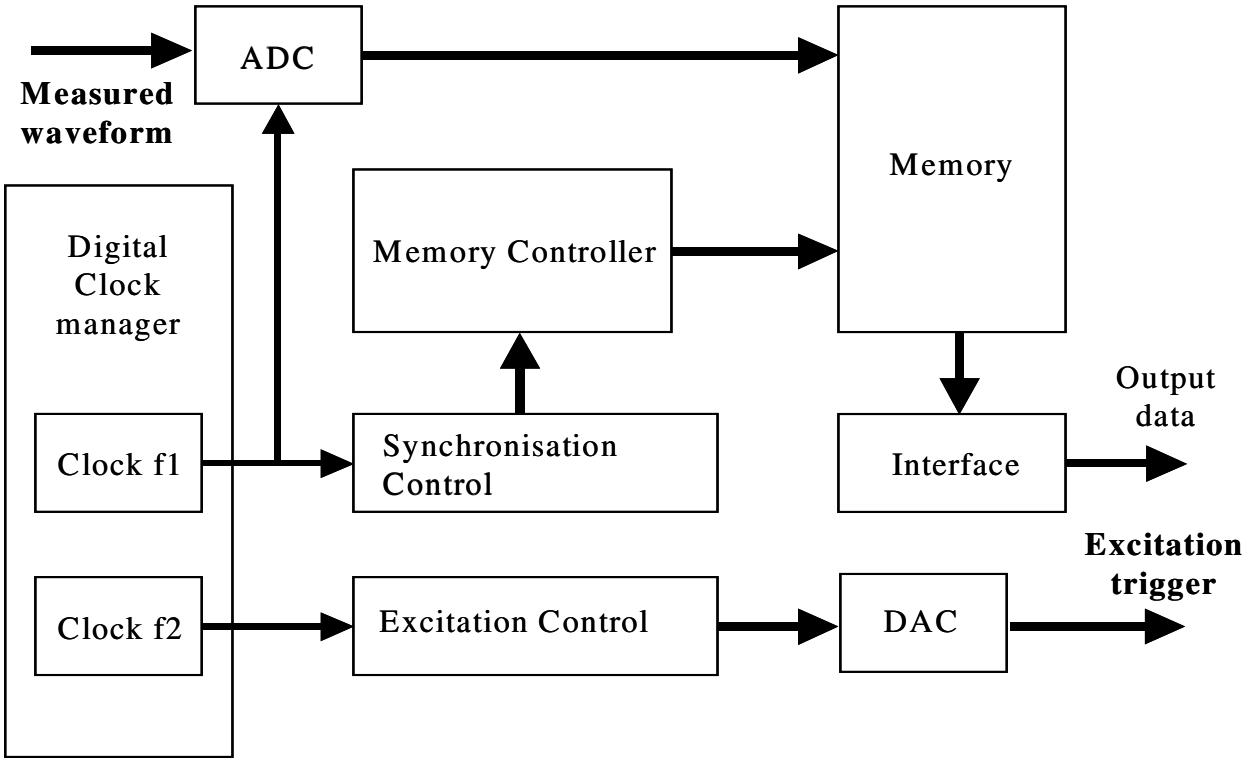

Fig.3. Block diagram of two clock timing architecture

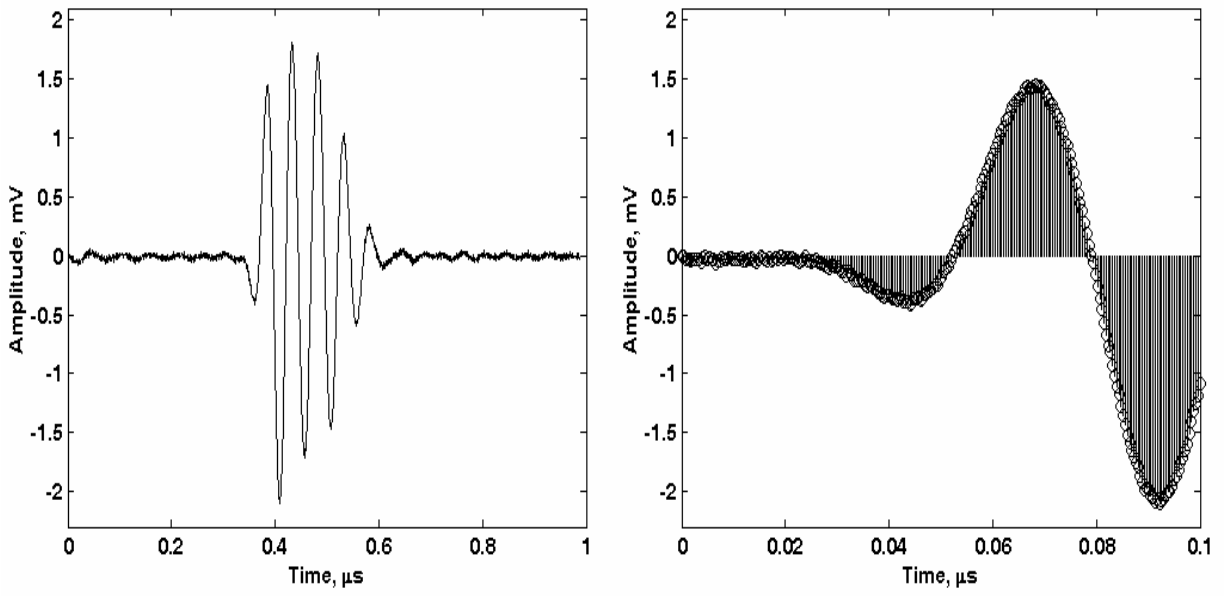

Fig.4. Experimentally recorded ultrasonic signal (clock ratio 26/27, ADC frequency 80 MHz, equivalent sampling frequency 27*80=2160 MHz, 1024 averages, transducer central frequency 20 MHz)

synchronized with the basic frequency and produced by the DCM.

Fast prototyping tools are required for economic implementation of this type of architecture and so the design package should support a high level of abstraction, design verification features, and convenient external interfaces. To meet all of these requirements the Xilinx Xtreme DSP development kit was used (Xilinx, San Jose, USA), which included the following relevant hardware: two 14 bit ADCs with a rated sampling frequency of 65 Msps, two 14 bit DACs with a sampling rate of 160 Msps, reconfigurable Virtex-II FPGA chip containing 3,000,000 logic gates. The

kit includes System Generator software that is a plug-in facility for the MATLAB Simulink toolbox. The development kit was complemented by an ultrasonic pulser-receiver system (NDT Solutions Ltd, Chesterfield, UK) that provided the ultrasonic hardware front-end.

Because the System Generator could not control the on-chip DCMs mentioned earlier we linked the System Generator output VHDL code to a custom VHDL code that was primarily intended for the control of DCMs. The resulting code was subsequently imported as a black box back into the System Generator for use in hardware co-simulation. The block diagram of the design is presented in fig.3.

The size of the on-chip dual port RAM was the most restricting aspect of the system. At 32 bits width 16 x 1024 samples required in excess of 500k bits and demanded much of the resource of the FPGA. Key parameters for our system were a clock frequency ratio 26/27 which gave an equivalent sampling rate of 2160 MHz with the single ADC clocked at 80 MHz and the accompanying feature of averaging if required.

An example of an acquired waveform is presented in fig.4. We found that for monitoring of chemical reactions 256 averages improve the signal to noise ratio enough for subsequent processing. That ensured a total measurement time of less than 2 seconds for a pulse repetition frequency of 4 kHz. The number of averages could be reduced if, for example, a living organism is observed, to increase the frame rate. If no averaging is used, the frame rate for this repetition frequency could be up to 148 Hz.

The developed instrument is being used for monitoring of chemical reactions with a resolution of less than 100 ppm *in situ*, and was found essential for temperature compensation of raw ultrasonic records [12].

IV. DISCUSSION ON AIS POWER DISSIPATION

A growing importance of lowering power dissipation of commercial ADCs was identified a decade ago [13], and its significance was further highlighted in a recent review [14]. Frame interleaved sampling does require an ADC to operate for several frames rather than one that leads to a proportional increase in power dissipation. However lowering the operating sampling frequency that enables use of less power-hungry ADCs offsets this trend. In this section we examine theoretical limits analyzed in [15], present statistical trends for a huge set of commercially available ADCs [14], and consider some state-of-the-art ADCs for a particular design.

Theoretical considerations led to the conclusion that the power dissipation of the sample-and-hold stage of an ADC P_{diss} is at least proportional to the sampling frequency [15]. An analysis of commercially available products (that incorporate comparators, error correction and other additional circuits) showed the following expression holds at present [14]:

$$P_{diss} = k f_s^{1.1} \tag{3}$$

where parameter k is dependent on an ADC's structure, resolution etc. A figure of merit F was used to quantify the energy efficiency of an ADC [13,14], but it can be simplified to become more convenient (in terms of physical sense and range of values) in this analysis. The dissipation energy per sample (*EPS*) can be expressed as follows

$$EPS = P_{diss}\Delta t = \frac{P_{diss}}{f_s} = \frac{F}{2^N}, \tag{4}$$

where N is the number of bits. AIS involves proportional increase in both equivalent sampling frequency and power consumption thus, using (3),

$$EPS_{AIS} = \frac{M_1 \times P_{diss}}{M_1 \times f_s} = \frac{P_{diss}}{f_s} = \frac{k f_s^{1.1}}{f_s} = k f_s^{0.1}, \tag{5}$$

which is independent of M_1. Therefore the EPS value specific to a particular ADC can be directly used for comparison of energy efficiency for AIS among ADCs with different maximal sampling frequencies. If this notional ADC was scaled towards the higher sampling frequencies by a factor of M_1, its EPS would become

$$EPS_{scaled} = \frac{P_{diss\ scaled}}{f_{s\ scaled}} = \frac{k(M_1 f_s)^{1.1}}{M_1 f_s} = k(M_1 f_s)^{0.1}. \tag{6}$$

The ratio of (5) and (6) yields

$$\frac{EPS_{scaled}}{EPS_{AIS}} = M_1^{0.1} > 1 \quad \forall \quad M_1 > 1. \tag{7}$$

For example, using a slower ADC and 10 frames instead of a fast ADC will reduce required energy per sample to $10^{0.1} \approx 1.25$ times (by 25%). This shows that AIS is more energy efficient than faster ADCs as indicated by the contemporary set of commercially available ADCs analyzed in [14]. Both architectures would approach the same efficiency (or wastefulness) if the power dissipation was determined by the sample-and-hold part of ADCs solely.

The above analysis is not applicable directly to the choice of ADC that an instrument designer faces. Specific ADCs differ in power consumption due to differences in ADC structure and manufacturing tolerances, package, output options (e.g., LVDS, parallel, serial) etc. We analysed offerings from one vendor (Analog Devices [15]) that are capable of achieving 200 MHz sampling frequency directly or through AIS, with the same resolution (12 bits), output (parallel) and minimal power dissipation for every maximal sampling frequency. The EPS values are presented in fig5. This plot illustrates that the 20 MHz ADC is a clear winner for this application (that is compatible with above considerations), although the latest device (AD9430) outperforms slightly most of the older designs. Using EPS in nJ as a quantitative measure enables a wide range of ADCs to be presented on a linear (rather than logarithmic) scale within a convenient range of 5..15 nJ. This facilitates unambiguous comparison of different ADCs for AIS.

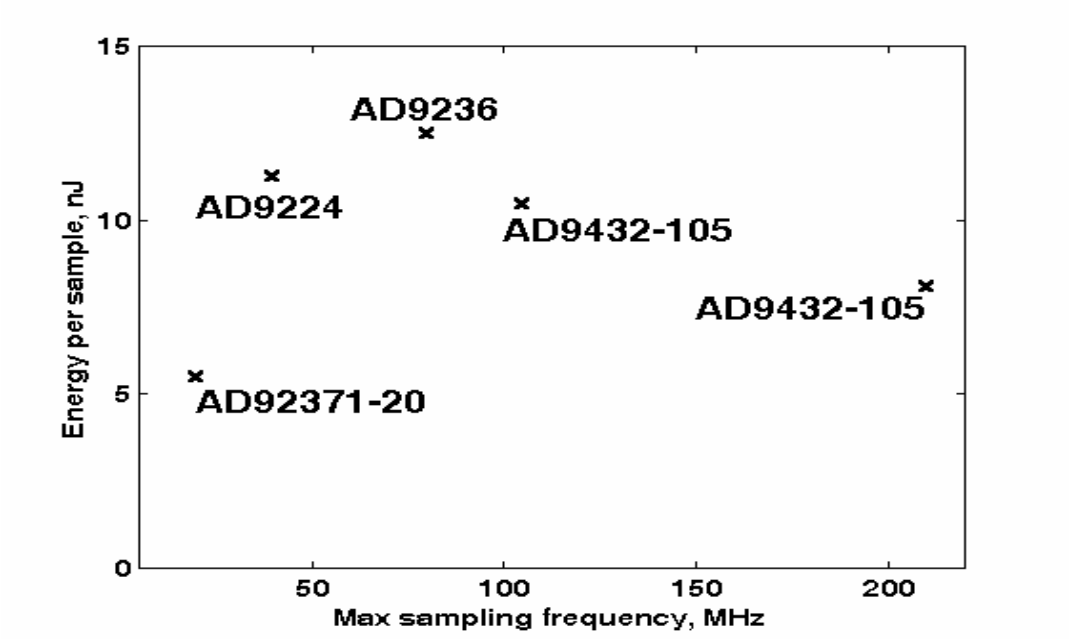

Fig.5. Energy per sample values for different ADCs

Moreover, the above analysis is applicable to ADC interleaving as well. For example, ADC interleaving using ten AD92371-20 operating at 20 MHz instead of a single AD92371-20 operating at 200 MHz would be more energy efficient. That is because these ADCs will deliver the same number of samples as the single AD9432-105, but they require less energy per sample (as seen from fig.5).

V. CONCLUSIONS

This paper shows that it is possible to trade off temporal resolution with measurement time by using frame interleaving with a single low speed ADC. Using a minimal number of frames (repetitions) requires accurate synchronization between the excitation of the waveform of interest and the ADC employed. It is shown how this synchronization could be achieved by using two linked oscillators inside a commercially available FPGA, providing an equivalent sampling frequency well beyond the capabilities of any element involved in the design. The approach provides significant cost and some power consumption advantages over other architectures if it is applicable. We applied this technique to ultrasonic instrumentation (e.g., [12]), and it can be further used for medical imaging, radar, sonar and other applications provided the waveform of interest could be excited repeatedly at will.

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